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|  |  |  |  |  |  | Załącznik nr 2 do Zarządzenia Nr 915 z 2019 r. Rektora PB | | | | |
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|  |  |  |  | **COURSE DESCRIPTION CARD** | | | |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
| **Faculty of Electrical Engineering** | | | | | | | | | | |
| **Field of study** | **Electrical and Electronic Engineering** | | | | | | | **Degree level and programme type** | **Bachelor's degree** | |
| **Specialization/ diploma path** | **-** | | | | | | | **Study profile** | **-** | |
| **Course name** | **Field Programmable Gate Arrays** | | | | | | | **Course code** | **IS-FEE-10031S** | |
| **Course type** | **elective** | |
| **Forms and number of hours of tuition** | **L** | **C** | **LC** | **P** | **SW** | **FW** | **S** | **Semester** | **summer** | |
| **15** |  | **30** |  |  |  |  | **No. of ECTS credits** | **5** | |
| **Entry requirements** |  | | | | | | | | | |
| **Course objectives** | The target of this course is to introduce the students to the structural design of FPGAs in the way, which is appropriate for both programmers and hardware engineers. | | | | | | | | | |
| **Course content** | Internal FPGAs architecture, clock signal frequency synthesis, signal I/O standards. CAD software for designing FPGAs - Intel Quartus II software. Design flow of FPGAs. VHDL: fundamentalunits, librarydeclarations, entity, architecture. Concurrent code. Sequential code.State machines. Packages and components. Functions and procedures. IEEE standard packages. Techniques description of the project, simulation, implementation and programming of FPGAs. Constructing a digital circuit using FPGAs. Synthesis of complex hierarchical designs. Synthesis of digital systems using standard prototype modules. Support for external devices via FPGA: PWM signal modulation, I2C and SPI bus control. | | | | | | | | | |
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| **Teaching methods** | describes the basic features and properties of FPGAs, | | | | | | | | | |
| **Assessment method** | **lecture – test, laboratory classes – evaluation of reports** | | | | | | | | | |
| **Symbol of learning outcome** | **Learning outcomes** | | | | | | | | **Reference to the learning outcomes for the field of study** | |
| **LO1** | describes the basic features and properties of FPGAs, | | | | | | | |  | |
| **LO2** | recognizes the syntax of the VHDL statements, | | | | | | | |  | |
| **LO3** | uses the features of the CAD FPGA platform, | | | | | | | |  | |
| **LO4** | designs simple digital systems in programmable structures, | | | | | | | |  | |
| **LO5** | uses VHDL to describe the system and designs new components, | | | | | | | |  | |
| **LO6** | combines various description techniques to design complex systems, | | | | | | | |  | |
| **LO7** | can run a simple digital system using conventional prototype modules. | | | | | | | |  | |
| **LO8** |  | | | | | | | |  | |
| **Symbol of learning outcome** | **Methods of assessing the learning outcomes** | | | | | | | | **Type of tuition during which the outcome is assessed** | |
| **LO1** | evaluating the student's test | | | | | | | | **L** | |
| **LO2** | evaluating the student's test | | | | | | | | **L** | |
| **LO3** | evaluating the student's reports | | | | | | | | **LC** | |
| **LO4** | evaluating the student's reports | | | | | | | | **LC** | |
| **LO5** | evaluating the student's reports | | | | | | | | **LC** | |
| **LO6** | evaluating the student's reports | | | | | | | | **LC** | |
| **LO7** | evaluating the student's reports | | | | | | | | **LC** | |
| **LO8** |  | | | | | | | |  | |
| **Student workload (in hours)** | | | | | | | | | **No. of hours** | |
| **Calculation** | **lecture attendance** | | | | | | | | **15** | |
| **participation in laboratory classes** | | | | | | | | **30** | |
| **preparation for laboratory classes** | | | | | | | | **30** | |
| **working on reports** | | | | | | | | **25** | |
| **participation in student-teacher sessions related to the classes and laboratory classes** | | | | | | | | **5** | |
| **preparation for and participation in test** | | | | | | | | **20** | |
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| **TOTAL:** | | | | | | | | **125** | |
| **Quantitative indicators** | | | | | | | | | **HOURS** | **No. of ECTS credits** |
| **Student workload – activities that require direct teacher participation** | | | | | | | | | **47** | **1,5** |
| **Student workload – practical activities** | | | | | | | | | **102** | **4** |
| **Basic references** | 1. Floyd L. T.: Digital Fundamentals with PLD Programming, Prentice Hall, 2005 2. Volnei A. Pedroni: Circuit Design with VHDL, MIT, Cambridge, London, 2004 3. Jha N.K., Gupta S.: Testing of Digital Systems, Cambridge University Press, 2003 4. IEEE Standard 1076-2008 VHDL-200X 5. Hamblen J., Hall T., Furman M.: Rapid Prototyping of Digital Systems, Springer, 2008 | | | | | | | | | |
| **Supplementary references** | 1. Terasic Inc.: DE2-115 User Manual, www.terasic.com, 2010 2. My First FPGA for Altera DE2-115 Board, www.terasic.com, 2010 3. My First Nios II for Altera DE2-115 Board, www.terasic.com, 2010 4. Pedroni V.: Circuit Design with VHDL, MIT Press, 2004 5. Hwang E. - ELECTRONiX: Digital Logic and Microprocessor Design with VHDL, La Sierra University, 2005 | | | | | | | | | |
| **Organisational unit conducting the course** | **Department of Automatic Control and Robotics** | | | | | | | | **Date of issuing the programme** | |
| **Author of the programme** | **Marian Gilewski, Ph.D. Eng.** | | | | | | | | **31.01.2020** | |
| **L – lecture, C – classes, LC – laboratory classes, P – project, SW – specialization workshop, FW - field work, S – seminar** | | | | | | | | | |  |