# COURSE DESCRIPTION CARD

| Faculty of Electrical Engineering | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Field of study | Electrical and Electronics Engineering | | | | | | | Degree level and programme type | bachelor's degree, full time programme |
| Specialization/ diploma path | - | | | | | | | Study profile | - |
| Course name | Workshop on Programmable Logic Device | | | | | | | Course code | IS-FEE-10038S |
| | | | | | | | | Course type | elective |
| Forms and number of hours of tuition | L | C | LC | P | SW | FW | S | Semester | summer |
| | | | | | 30 | | | No. of ECTS credits | 4 |
| Entry requirements | - | | | | | | | | |
| Course objectives | Use of programmable logic device in real life example. Preparation of technical documentation, tools description and programming methods. Use of hardware description language to synthesise logic device controlling assigned plant. Oral presentation with discussion on individual project. | | | | | | | | |
| Course content | Programmable logic device (PLD) especially field programmed gate array (FPGA) characterisation. Introduction to selected computer-aided design (CAD) tool and hardware description language (HDL). Programming and testing of logic devices based on standard and self-prepared libraries. Automatic control of selected peripheral device. Synthesis of real life example of logic devise based on FPGA modul. | | | | | | | | |
| Teaching methods | project/specialization workshop. | | | | | | | | |
| Assessment method | projects completion, presentation and discussion of the projects. | | | | | | | | |

| Symbol of learning outcome | Learning outcomes<br>*After completing this subject student is able to:* | Reference to the learning outcomes for the field of study |
|---|---|---|
| LO1 | characterize programmable logic devices; | |
| LO2 | gather information from technical documentation; | |
| LO3 | prepare his own technical documentation; | |
| LO4 | presents problems and solutions concerning assigned project; | |
| LO5 | use necessary programming tools; | |
| LO6 | use selected hardware description language; | |
| LO7 | identify time and funds necessary for project realization; | |
| LO8 | work well individually and in a group. | |

| Symbol of learning outcome | Methods of assessing the learning outcomes | Type of tuition during which the outcome is assessed |
|---|---|---|
| LO1 | project documentation and oral presentation; | |
| LO2 | project documentation; | |

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| LO3 | initial project documentation; | |
| LO4 | oral presentation; | |
| LO5 | project documentation; | |
| LO6 | project documentation; | |
| LO7 | project documentation; | |
| LO8 | discussion of the student's projects, evaluation of the student's performance in classes | |
| Student workload (in hours) | | No. of hours |
| Calculation | participation in classes | 30 |
| | preparation for classes | 15 |
| | work on projects | 60 |
| | participation in student-teacher sessions related to the class | 1 |
| | preparation for and participation in project presentations | 6 |
| | | |
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| | | |
| | TOTAL: | 112 |

| Quantitative indicators | HOURS | No. of ECTS credits |
|---|---|---|
| Student workload – activities that require direct teacher participation | 30 | 1 |
| Student workload – practical activities | 112 | 4 |

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| Basic references | 1. Deschamps J. P.: Synthesis of arithmetic circuits FPGA, ASIC and embedded systems. J. Wiley, 2006.<br>2. Chu P. P.: FPGA prototyping by VHDL examples: Xiling Spartan-3 version. J. Wiley, 2008.<br>3. http://www.altera.com/literature/lit-index.html | |
| Supplementary references | 1. http://www.fpga4fun.com/ | |
| Organisational unit conducting the course | Department of Automatic Control and Robotics | Date of issuing the programme |
| Author of the programme | Łukasz Sajewski, Ph.D. Eng. | 08.02.2020 |

L – lecture, C – classes, LC – laboratory classes, P – project, SW – specialization workshop, FW - field work,

S – seminar